Dual 2-Input NAND Gate

The NLX2G00 is an advanced high-speed dual 2-input CMOS NAND gate in ultra-small footprint.

The NLX2G00 input structures provide protection when voltages up to 7.0 volts are applied, regardless of the supply voltage.

Features

- High Speed: t_{PD} 2.4 ns (typical) at $V_{CC} = 5.0 \text{ V}$
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Low Power Dissipation: $I_{CC} = 1 \mu A$ (Max) at $T_A = 25^{\circ}C$
- 24 mA Balanced Output Sink and Source Capability
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input Pins
- This is a Pb-Free Device

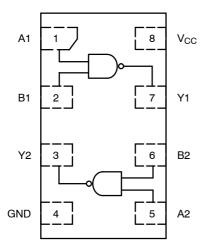


Figure 1. Pinout

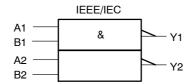


Figure 2. Logic Symbol



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MARKING DIAGRAMS



ULLGA8 1.45 x 1.0 CASE 613AA





ULLGA8 1.6 x 1.0 CASE 613AB





ULLGA8 1.95 x 1.0 CASE 613AC

AHM ○ ■

XX M

= Specific Device Code

= Date Code

= Pb-Free Package

PIN ASSIGNMENT

Pin	Function
1	A1
2	B1
3	Y2
4	GND
5	A2
6	B2
7	Y1
8	V _{CC}

FUNCTION TABLE

 $Y = \overline{AB}$

Inp	Output	
Α	В	Υ
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

H = HIGH Logic Level

L = LOW Logic Level

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current V _{IN} < GND	-50	mA
I _{OK}	DC Output Diode Current V _{OUT} < GND	-50	mA
Io	DC Output Source/Sink Current	±50	mA
I _{CC}	DC Supply Current per Supply Pin	±100	mA
I _{GND}	DC Ground Current per Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	TBD	°C
TJ	Junction Temperature Under Bias	TBD	°C
$\theta_{\sf JA}$	Thermal Resistance (Note 1)	TBD	°C/W
P_{D}	Power Dissipation in Still Air at 85°C	TBD	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I _{Latchup}	Latchup Performance Above V _{CC} and Below GND at 125°C (Note 5)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
- 2. Tested to EIA/JESD22-A114-A.
- 3. Tested to EIA/JESD22-A115-A.
- 4. Tested to JESD22-C101-A.
- 5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Power DC Supply Voltage	Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V _{IN}	Digital Input Voltage (Note 6)		0	5.5	V
V _{OUT}	Output Voltage		0	V _{CC}	V
T _A	Operating Free-Air Temperature		-55	+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate	$V_{CC} = 1.8 \text{ V } \pm 0.15 \text{ V}$ $V_{CC} = 2.5 \text{ V } \pm 0.2 \text{ V}$ $V_{CC} = 3.3 \text{ V } \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V } \pm 0.5 \text{ V}$	0 0 0	20 20 10 5	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

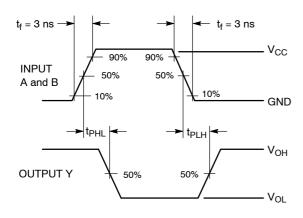
DC ELECTRICAL CHARACTERISTICS

			V _{CC}	T _A = 25°C		T _A = 25°C		T _A = 25°C		T _A = 25°C		T _A = 25°C		T _A = 25°C		T _A = -55°C to T _A ≤ 85°C +125°C			
Symbol	Parameter	Condition	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit								
V _{IH}	High-Level Input Voltage		1.65 2.3 to 5.5	0.75 x V _{CC} 0.7 x V _{CC}			0.75 x V _{CC} 0.7 x V _{CC}		0.75 x V _{CC} 0.7 x V _{CC}		V								
V _{IL}	Low-Level Input Voltage		1.65 2.3 to 5.5			0.25 x V _{CC} 0.3 x V _{CC}		0.25 x V _{CC} 0.3 x V _{CC}		0.25 x V _{CC} 0.3 x V _{CC}	V								
V _{OH}	High-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $I_{OH} = -100 \mu A$	1.65 to 5.5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V _{CC} - 0.1		V								
		$\begin{aligned} &V_{IN} = V_{IH} \text{ or } V_{IL} \\ &I_{OH} = -4 \text{ mA} \\ &I_{OH} = -8 \text{ mA} \\ &I_{OH} = -12 \text{ mA} \\ &I_{OH} = -16 \text{ mA} \\ &I_{OH} = -24 \text{ mA} \\ &I_{OH} = -32 \text{ mA} \end{aligned}$	1.65 2.3 2.7 3.0 3.0 4.5	1.29 1.9 2.2 2.4 2.3 3.8	1.5 2.1 2.4 2.7 2.5 4.0		1.29 1.9 2.2 2.4 2.3 3.8		1.29 1.9 2.2 2.4 2.3 3.8										
V _{OL}	Low-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $I_{OL} = 100 \mu A$	1.65 to 5.5			0.1		0.1		0.1	٧								
		$\begin{aligned} &V_{IN} = V_{IH} \text{ or } V_{IL} \\ &I_{OL} = 4 \text{ mA} \\ &I_{OL} = 8 \text{ mA} \\ &I_{OL} = 12 \text{ mA} \\ &I_{OL} = 16 \text{ mA} \\ &I_{OL} = 24 \text{ mA} \\ &I_{OL} = 32 \text{ mA} \end{aligned}$	1.65 2.3 2.7 3.0 3.0 4.5		0.08 0.20 0.22 0.28 0.38 0.42	0.24 0.3 0.4 0.4 0.55 0.55		0.24 0.3 0.4 0.4 0.55 0.55		0.24 0.3 0.4 0.4 0.55 0.55									
I _{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5 \text{ V}$	0 to 5.5			±0.1		± 1.0		±1.0	μΑ								
I _{OFF}	Power-Off Input Leakage Current	V _{IN} = 5.5 V	0			1.0		10		10	μΑ								
Icc	Quiescent Supply Current	$0 \le V_{IN} \le 5.5 \text{ V}$	5.5			1.0		10		10	μΑ								

AC ELECTRICAL CHARACTERISTICS t_{R} = t_{F} = 2.5 ns

		V _{CC}		т	A = 25°	С	T _A ≤	85°C	_ ~	-55°C 25°C	
Symbol	Parameter	(V)	Test Condition	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH}	Propagation Delay	1.65 to 1.95	$R_L = 1 \text{ M}\Omega, C_L = 15 \text{ pF}$	2.0	5.7	10.5	2.0	11.0	TBD	TBD	ns
t _{PHL}	Input A to Output	2.3 to 2.7	$R_L = 1 \text{ M}\Omega, C_L = 15 \text{ pF}$	1.2	3.2	5.3	1.2	5.7	TBD	TBD	
		3.0 to 3.6	$R_L = 1 M\Omega$, $C_L = 15 pF$	0.8	2.4	3.7	0.8	4.0	TBD	TBD	
			$R_L = 500 \ \Omega, C_L = 50 \ pF$	1.2	3.0	4.6	1.2	4.9	TBD	TBD	
		4.5 to 5.5	$R_L = 1 \text{ M}\Omega, C_L = 15 \text{ pF}$	0.5	1.9	2.9	0.5	3.2	TBD	TBD	
			$R_L = 500 \ \Omega, C_L = 50 \ pF$	0.8	2.4	3.6	0.8	3.9	TBD	TBD	
C _{IN}	Input Capacitance	5.5	V _{IN} = 0 V or V _{CC}		2.5						pF
C _{PD}	Power Dissipation Capacitance (Note 7)	3.3 5.5	10 MHz, V _{IN} = 0V or V _{CC}		9 11						pF

^{7.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.



INPUT OUTPUT

A 1–MHz square input wave is recommended for propagation delay tests.

Figure 3. Switching Waveform

Figure 4. Test Circuit

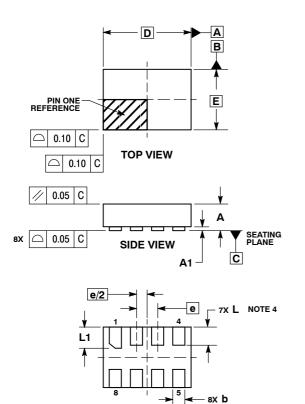
ORDERING INFORMATION

Device	Package	Shipping [†]
NLX2G00AMX1TCG	ULLGA8, 1.95 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX2G00BMX1TCG	ULLGA8, 1.6 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX2G00CMX1TCG	ULLGA8, 1.45 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

ULLGA8 1.45x1.0, 0.35P CASE 613AA-01 ISSUE A



BOTTOM VIEW

0.10 C A B

0.05 C NOTE 3

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- NOTES:

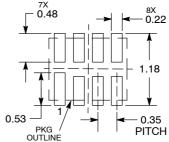
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: MILLIMETERS.

 3. DIMENSION 6 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
- 4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

	MILLIMETERS					
DIM	MIN	MAX				
Α		0.40				
A 1	0.00	0.05				
b	0.15	0.25				
D	1.45 BSC					
Е	1.00 BSC					
e	0.35 BSC					
Ĺ	0.25	0.35				
L1	0.30	0.40				

MOUNTING FOOTPRINT SOLDERMASK DEFINED*

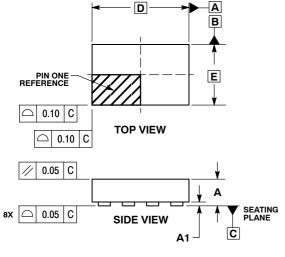


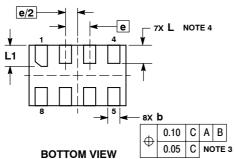
DIMENSIONS: MILLIMETERS

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

ULLGA8 1.6x1.0, 0.4P CASE 613AB-01 **ISSUE A**

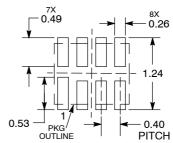




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
 4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED. PACKAGE IS ALLOWED.

	MILLIMETERS							
DIM	MIN	MAX						
Α		0.40						
A1	0.00	0.05						
b	0.15	0.25						
D	1.60	BSC						
E	1.00 BSC							
е	0.40 BSC							
L	0.25	0.35						
L1	0.30	0.40						

MOUNTING FOOTPRINT SOLDERMASK DEFINED*

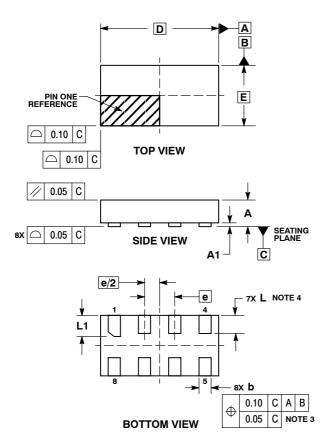


DIMENSIONS: MILLIMETERS

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

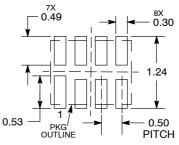
ULLGA8 1.95x1.0, 0.5P CASE 613AC-01 **ISSUE A**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
 - ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
- A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

	MILLIMETERS							
DIM	MIN	MAX						
Α		0.40						
A1	0.00	0.05						
b	0.15	0.25						
D	1.95 BSC							
Е	1.00 BSC							
е	0.50 BSC							
L	0.25	0.35						
L1	0.30	0.40						

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

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